ABSTRACT OF THE DISCLOSURE

A test apparatus for a semiconductor device, which improves the reliability of an operational test on target devices on a wafer using BOST (Built Out Self Test) and BIST (Built In Self Test). The test apparatus includes an external test unit, the BIST circuit formed in the semiconductor device, and BOST device which is coupled between the external test unit and the semiconductor device. Pattern data for a pattern dependency test is stored in the BIST circuit and pattern data for a timing dependency test is stored in the BOST device.